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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/845,405	04/30/2001	Gerhard Beitel	GR 00 P 4091	2869

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EXAMINER

VINH, LAN

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 10/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/845,405

Applicant(s)

BEITEL ET AL.

Examiner

Lan Vinh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 April 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 09/845,405.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6,7,9.
- ☐ Interview Summary (PTO-413) Paper No(s). _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

Information Disclosure Statement

1. The document 0901 157 A2 listed in the Information Disclosure Statement filed on 6/14/2001 (paper no. 7) has not been considered because there is no English translation for the document. It has been placed in the application file, but the information referred to therein has not been considered as to the merits.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1-2, 4, 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Morgan (US 6,180,525)

Morgan discloses a method for minimizing repetitive chemical mechanical polishing scratch marks from occurring on a polished semiconductor wafer. This method comprises the steps of:

providing a substrate 12 having a structure 32, the structure 32 is removed during a subsequent step (col 3, lines 40-55)

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forming/depositing a sacrificial layer 40 on the structure 32 and substrate 12 (col 4, lines 49-51; fig.6)

removing the sacrificial layer 40 and structure 32 in a chemical mechanical polishing step (col 4, lines 47-49)

Regarding claim 2, Morgan discloses that the structure 32 is made of insulating/dielectric material (col 4, lines 10-11)

The limitation of claim 4 has been discussed above

Regarding claim 5, Morgan discloses that sacrificial layer 40 can comprise the same material as layer 32, layer 32 is a deposited oxide/silicon oxide (col 3, lines 57-58; col 4, lines 36-37)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morgan (US 6,180,525) in view of Paranjpe (US 5,434,107)

Morgan's method has been described above in paragraph 3. Unlike the instant claimed inventions as per claims 3, 7, Morgan does not disclose the specific aspect ratio during the removing step by polishing.

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However, Paranipe, in a method for planarization by polishing, teaches that the polishing/removing rates are a function of many variables including aspect ratio, material type (col 2, lines 44-46)

Hence, one skilled in the art would have found it obvious to modify Morgan's polishing method by changing the variable of aspect ratio through conducting routine experimentation to obtain any specific value of aspect ratio in order to achieve a desired polishing rate.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morgan (US 6,180,525) in view of Ismail et al (US 5,955,759)

Morgan's method has been described above in paragraph 3. Unlike the instant claimed inventions as per claim 6, Morgan fails to disclose the step of removing residue of the sacrificial layer by wet processes followed the CMP.

However, Ismail discloses a method for manufacturing a semiconductor device using CMP comprises the step of removing the remaining sacrificial layer 1 by wet etching (col 3, line 48-49)

Hence, one skilled in the art would have found it obvious to modify Morgan method by adding the step of removing the remaining sacrificial layer 1 by wet etching as per Ismail after the CMP step because Ismail teaches that sacrificial layer is preferably removed by wet etching to avoid reactive ion etching damage to the semiconductor structure (col 3, lines 49-50)

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7. Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chien et al (US 5,702,869) in view of Huff et al (US 5,872,401)

Chien discloses a method for removing photoresist from a semiconductor substrate.

This method comprises the steps of:

providing a substrate 10 (col 5, lines 53-54)

forming one layer 32 on the substrate, layer 32 is patterned and etched to form patterned layer 32a/ semiconductor structure (fig. 7)

forming a photoresist layer/ mask to layer 32 (col 11, lines 56-57)

etching layer 32 by RIE/dry etching process, the residues 35a formed at the sidewall of the resist/mask layer (col 11, lines 45-66, fig. 7) reads on etching the layer being structured by a dry etching method, so that redepositions of the layer emerge at sidewalls of the mask

removing the resist layer/mask layer (col 12, lines 19-21)

performing a planarizing/polishing step (col 11, lines 32-36)

Unlike the instant claimed invention as per claim 8, Chien does not specifically disclose the steps of applying a sacrificial layer and performing a polishing step to remove the residues/redeposition and the sacrificial layer so that a structured layer emerges.

However, Huff discloses a method of forming a semiconductor structure comprises the steps of applying a sacrificial layer 390 (silicon oxide) and performing a polishing step to remove the redeposition 370 and the sacrificial layer 390 to form an emerging layer 400 (col 6, lines 1-11)

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Since both Chien and Huff are concerned with method of making semiconductor structure using CMP, one skilled in the art would have found it obvious to modify Chien by adding the steps of applying a sacrificial layer and performing a polishing step to remove the residues/redeposition and the sacrificial layer as per Huff because Huff teaches that the sacrificial layer make the interlevel dielectric layer compressive and the planarization/polishing removes the excess oxide of the sacrificial layer and creates a very level surface for further processing (col 5, lines 15-18, col 6, lines 11-14)

Regarding claim 9, Chien discloses forming the layer 32 of dielectric material (col 11, lines 45-46)

Regarding claim 10, Chien discloses removing the residues 35a' from the resist/mask and stopping the polishing step (col 7, lines 17-22; col 12, lines 40-42)

Regarding claim 11, Chien discloses performing the polishing step using CMP (col 7, line 17)

The limitation of claim 12, forming the sacrificial layer of silicon oxide, has been described above.

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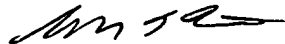
Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302.

The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.



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LV
September 27, 2002